AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application

Applicant(s): Fratti et al.
Case: Fratti 12-19
Serial No.: 10/628,941
Filing Date: July 29, 2003
Group: 2811
Examiner: Thomas J. Magee

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Date: June 27, 2005

Title: Techniques for Curvature Control in Power Transistor Devices

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APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated January 21, 2005 of claims 1-16 of the above-identified application.

REAL PARTY IN INTEREST

The present application is currently assigned to Agere Systems Inc. Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

Claims 1-16 are pending in the above-identified patent application. Claims 1, 13 and 16 are the independent claims.

Each of claims 1-16 stands finally rejected under 35 U.S.C. §103(a). Claims 1-16 are appealed.

STATUS OF AMENDMENTS

There have been no amendments to the claims filed subsequent to the appealed rejections.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to techniques for processing power transistor devices. See, Specification, page 1, lines 25-26.

According to one exemplary embodiment of the invention, a method for controlling curvature of a power transistor device, having a device film formed on a substrate, is provided (Specification, page 1, lines 26-28). The method comprises the following steps. The substrate is thinned and the device has an overall residual stress attributable at least in part to the thinning of the substrate (Specification, page 1, lines 28-29). A stress compensation layer is applied to a surface of the device film which has a tensile stress sufficient to counterbalance at least a portion of the overall residual stress of the device (Specification, page 1, lines 29-31).

According to another exemplary embodiment of the invention, a power transistor device having a substrate and a device film formed on the substrate is provided (Specification, page 2, line 3). The power transistor device has an overall residual stress attributable at least in part to a thinning process applied to the substrate (Specification, page 2, line 5). The power transistor device has a stress compensation layer formed on a surface of the device film which has a tensile stress that counterbalances at least a portion of the overall residual stress of the device (Specification, page 2, lines 5-8).

According to yet another exemplary embodiment of the invention, the power transistor device is part of an integrated circuit (Specification, page 2, lines 8-9).

An illustrative embodiment of the invention is shown in FIG. 4 of the drawings, wherein DMOS device 100 comprises DMOS film 102 and substrate 104 (Specification, page 8, lines 15-17). Aggressive backside substrate removal processing is employed to thin substrate 104, which reduces the tensile stress of substrate 104 relative to DMOS film 102 (Specification, page 8, lines 17-19). As a result of the processing, DMOS device 100 curves (Specification, page 8, line 19).

The stress of DMOS film 102 less the stress of substrate 104, which dictates the curvature of DMOS device 100, represents an overall stress in DMOS device 100 (Specification, page 8, lines 24-25). The overall residual stress should be counterbalanced, at least in part, to reverse, substantially eliminate, or prevent further curvature of DMOS device 100 (Specification, page 8, lines 28-29).

Thin film 410, e.g., a stress compensation layer, may be applied to a surface of DMOS device 100 over DMOS film 102 and opposite substrate 104 (Specification, page 9, lines 1-2 and 7-8). Thin film 410 has a tensile stress that counterbalances at least a portion of the overall residual stress of DMOS device 100 and renders DMOS device 100 flat, or slightly convex (Specification, page 9, lines 2-4).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-8 and 13-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,091,110 issued to Hebert et al. (hereinafter "Hebert") in view of U.S. Patent 6,162,665 issued to Zommer (hereinafter "Zommer") and further in view of S. Savastiouk et al., "Atmospheric Downstream Plasma," (hereinafter "Savastiouk").

2. Claims 9-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hebert in view of Zommer, Savastiouk and A. Sherman, "Chemical Vapor Deposition for Microelectronics," (hereinafter "Sherman"), and further in view of Wilson et al., "Handbook of Multilevel Metallization for Integrated Circuits," (hereinafter "Wilson").

ARGUMENT

1. §103(a) Rejection of Claims 1-8 and 13-16

Claims 1-6 and 8

Applicants initially note that M.P.E.P. §2143 indicates that establishing a *prima facie* case of obviousness requires that the following three criteria are met:

> [f]irst, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness for at least the reason that there exists no motivation to combine the references, and further, even if combinable, the references collectively do not teach each and every limitation of independent claim 1.

Independent claim 1 is directed to a method for controlling curvature of a power transistor device having a device film formed on a substrate. The method includes thinning the substrate and the device having an overall residual stress attributable, at least in part, to the thinning. A stress compensation layer is applied to a surface of the device film. The stress compensation layer has a tensile stress sufficient to counterbalance at least a portion of the overall residual stress of the device.

The Examiner, beginning on page 2, 3rd paragraph of the final Office Action, stated that,

> Hebert discloses a method for controlling the curvature (and stress) of a device, wherein a thin stress compensation layer, is formed on a substrate over the surface of the device. . . Hebert does not disclose thinning of the substrate or that the overall stress is attributable at least in part to the thinning step. Zommer discloses that the breakdown voltage is altered by changing the thickness of the substrate to alter resistivity by aggressive backsurface grinding, polishing, or thinning. Such techniques, however, are notoriously well known to introduce damage that will alter the residual stress (internal citations omitted).

The Examiner pointed to the teachings of Savastiouk to bolster the assertion that backsurface processing introduces damage that will alter residual stress.

Applicants respectfully disagree with the Examiner's assertions for at least the reason that there exists no motivation to combine the teachings of Hebert with those of Zommer and Savastiouk. For example, with regard to the proposed combination of Hebert and Zommer, the Examiner found it obvious to use the procedures of Zommer in Hebert "to obtain a backsurface thinned substrate with altered resistivity and breakdown voltage." See, final Office Action, page 3, 1st paragraph. The Examiner further concluded by reference to U.S. Patent 6,816,011 issued to Paul et al. (hereinafter "Paul") that "a higher breakdown voltage" (as allegedly achievable by the techniques of Zommer) is desirable. See, for example, Office Action, page 7, 4th paragraph.

Applicants disagree and respectfully submit that one of ordinary skill in the art would not be motivated to supplement the teachings of Hebert with those of Zommer to achieve "a higher

breakdown voltage," as the Examiner suggests, as it would be difficult to ascertain what actual breakdown voltage is present in Hebert and thus whether a relatively 'higher' breakdown voltage would even be desirable. For example, Hebert contains no substantive teachings regarding the substrate layer, e.g., P+ substrate layer 10 in FIG. 1. Therefore, it is the Applicants' position that one of ordinary skill in the art would not be motivated to combine the teachings of Hebert with those of Zommer.

In the Advisory Action, no further remarks were provided to bolster this position, other than on page 3, 2nd paragraph, wherein it was stated that "[t]he desirability of altering resistivity and threshold voltage is indeed a valid rationale [and] . . . other comments are not germane." Therefore, Applicants respectfully maintain their position that there exists no motivation to combine the teachings of the cited references.

Applicants respectfully further submit that the teachings of Hebert, Zommer and Savastiouk, even if combinable, in no way teach or suggest a stress compensation layer with a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of a power transistor device attributable, at least in part, to a thinning of a substrate of the device. Specifically, nothing in the combined teachings of the references in any way indicates that the dielectric layer of Hebert would have a tensile stress sufficient to counterbalance any amount of overall residual stress resulting from substrate thinning. For example, Hebert contains no teachings whatsoever regarding the purpose, function or any other substantive property of the oxide stress compensation layer. In fact, it appears from the limited teachings of Hebert that the stress compensation layer is merely present to compensate stresses inherent in layers adjacent thereto. For example, Hebert, at col. 2, beginning on line 54, teaches that the plasma enhanced CVD oxide layer (e.g., the stress relief layer) is deposited prior to a thick inter level dielectric being formed over it and the device being heated.

The Examiner seems to be taking the teachings of Hebert which, according to the Examiner's analysis, disclose a stress relief layer, and the teachings of Zommer which, according to the Examiner's analysis, disclose thinning of a substrate, and concluding that the layer in Hebert would be sufficient to counteract stress should thinning of the device in Hebert be performed as is taught in Zommer. This conclusion finds absolutely no support in any of the

cited teachings, absent use of the teachings of the present application as a guide, as the combined references do not in any way address counterbalancing stress from substrate thinning.

In the Advisory Action, page 2, 3rd paragraph, the Examiner further stated that, with regard to the above remarks,

> [c]omments of Applicant are not germane, since Hebert does indeed disclose a stress relief layer, Zommer does disclose thinning of the substrate. Additionally, the claim recites that 'a portion of the overall residual stress is [counterbalanced]' (internal citations omitted) (emphasis omitted).

Applicants respectfully submit that these remarks merely re-iterate the Examiner's previously made rejections. Therefore, Applicants maintain that the combined cited references do not teach or suggest counterbalancing overall residual stress attributable to substrate thinning.

The Examiner further stated, in the final Office Action, page 7, 3rd paragraph, that "it is notoriously well known that the deposition of a thin film oxide layer will cause a 'bending' or curvature." The Examiner makes reference to U.S. Patent No. 6,531,193 issued to Fonash et al. (hereinafter "Fonash"). Applicants, however, respectfully point out that with the lack of any specifics in Hebert regarding, e.g., the thickness of P+ substrate 10, it cannot be assumed, with any degree of certainty, that curvature occurs. For example, it is equally plausible, given the teachings in Hebert, that the P+ substrate is of a thickness such that no curvature is experienced.

Therefore, for at least the reasons stated above, Applicants respectfully submit that independent claim 1, as well as claims 2-6 and 8 dependent thereon, are patentable over Hebert in view of Zommer and Savastiouk.

Claim 7

With regard to claim 7, this claim specifies that the steps (e.g., of claim 1) of thinning the substrate and applying a stress compensation layer are performed repeatedly until a desired curvature is attained. Applicants respectfully submit that the teachings of the cited references, even if combinable, do not teach or suggest this limitation.

In the final Office Action, page 3, 6th paragraph, the Examiner stated that "Hebert and Zommer disclose . . . that the thinning of the substrate and application of a stress compensation layer produces a curvature of the device." The Examiner then concluded that "the 'repeated'

application would also produce a curvature and is therefore rejectable using the same criteria." See *Id.* The Examiner further stated in the Advisory Action, beginning on page 2, 4th paragraph, that "[w]ith regard to repeated applications of thinning and application of a stress compensation layer references for independent claim 1 are relevant and Svastiouk (sic.) et al. disclose that curvature is produced in the process of thinning, therefore repeated applications of the process will produce curvature." (internal citations omitted).

Applicants respectfully submit that these statements by the Examiner are incorrect. Hebert and Zommer do not disclose that thinning of the substrate would produce a curvature of the device as the Examiner contends. Hebert doesn't disclose curvature in a device or thinning of the substrate of a device. Zommer similarly makes absolutely no mention of curvature in a device. Savastiouk makes reference to wafer bowing and warping as being the result of "[e]arly backgrinding techniques [that] were crude." See, Savastiouk, page 1. Since neither Hebert nor Zommer are related to device curvature, and Savastiouk addresses bowing and warping negatively, it is implausible to find that the combined teachings would in any way relate to attaining a desired curvature.

Claims 13-15

Independent claim 13 is directed to a power transistor device having a substrate and a device film formed on the substrate. The device has an overall residual stress attributable at least in part to a thinning process applied to the substrate. The device further comprises a stress compensation layer formed on a surface of the device film. The stress compensation layer has a tensile stress that counterbalances at least a portion of the overall residual stress of the device.

In the final Office Action, beginning on page 4, 2nd paragraph, the Examiner stated that,

> [r]egarding Claims 13 and 16, Hebert discloses a power transistor device, wherein a thin film . . . is formed on a substrate as a stress compensation layer. Hebert does not disclose that the deposited oxide stress compensation layer has a tensile stress. However, Sherman discloses that the stress in the oxide film is tensile, wherein the tensile stress in the oxide film provides 'stress relief' in the device. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sherman with Hebert to obtain a film having tensile stress to relieve residual stress within the device.
>
> Additionally, Hebert does not disclose thinning of the substrate. Zommer discloses that the breakdown voltage is altered by changing the thickness of the

> substrate to alter resistivity by aggressive backsurface grinding, polishing, or thinning. Such techniques, however, are notoriously well known to introduce damage that will alter the residual stress. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Zommer in Hebert to obtain a backsurface thinned substrate with altered resistivity and breakdown voltage (internal citations omitted).

Applicants respectfully disagree with the Examiner's assertions for at least the reason that there exists no motivation to combine the cited references and that the references, even if combinable, do not teach each and every element of the claimed invention.

Applicants submit that, as stated above, there exists no motivation to combine the teachings of Hebert with those of Zommer. Specifically, Applicants assert that one of ordinary skill in the art would not be motivated to combine the teachings of Hebert with those of Zommer to "obtain a backsurface thinned substrate with altered resistivity and breakdown voltage," as the Examiner suggests, as it would be difficult to ascertain what actual breakdown voltage is present in Hebert, and thus whether altering the breakdown voltage would even be desirable. For example, as pointed out above, Hebert contains no substantive teachings regarding the substrate layer, e.g., P+ substrate layer 10 in FIG. 1.

Further, even if the cited references are combinable, they do not teach or suggest each and every element of the claimed invention. Applicants note that with regard to the stated grounds of rejection set forth on page 2, 2nd paragraph, of the final Office Action, no rejection of claims 1-8 and 13-16 is made based on Sherman. In the Advisory Action, page 2, 3rd paragraph, the Examiner stated that,

> Applicant is correct in noting that Sherman was omitted in the caption, but was recovered in the caption for Claims 9-12. However, assertions of patentability based on the independent claims . . . is not warranted (internal citations omitted).

It is still, however, unclear how the Examiner intended Sherman to apply to independent claim 13. Notwithstanding this ambiguity, Applicants respectfully submit that the combined teachings of Hebert, Zommer, Savastiouk and Sherman fail to teach or suggest each and every element present in independent claim 13.

Specifically, the combined teachings of Hebert, Zommer, Savastiouk and Sherman fail to teach or suggest a stress compensation layer that has a tensile stress that counterbalances at least

a portion of the overall residual stress of the device, the overall residual stress of the device being attributable at least in part to a thinning process applied to the substrate. For example, nothing in the combined teachings of the cited references in any way indicates that the tensile stress of an SiO_2 film, e.g., as taught in Sherman, combined with a stress relief dielectric layer, e.g., as taught in Hebert, would be able to counterbalance any amount of stress resulting from substrate thinning, e.g., as taught in Zommer. This element, absent in the cited references, is only taught in the present teachings.

Therefore, for at least the reasons stated above, independent claim 13, as well as claims 14 and 15 dependent thereon, are patentable over Hebert, Zommer, Savastiouk and Sherman. Reconsideration and withdrawal of the rejections is thus respectfully requested.

Claim 16

Independent claim 16 is directed to an integrated circuit having at least one power transistor device. The power transistor device has a substrate and a device film formed on the substrate. The device has an overall residual stress attributable at least in part to a thinning process applied to the substrate. The device further comprises a stress compensation layer formed on a surface of the device film. The stress compensation layer has a tensile stress that counterbalances at least a portion of the overall residual stress of the device.

As stated above, the Examiner rejected independent claim 16 over the combined teachings of Hebert, Zommer, Savastiouk and Sherman. Applicants respectfully disagree with the Examiner's assertions for at least the reasons that there exists no motivation to combine the cited references and that the references, even if combinable, do not teach each and every element of the claimed invention.

For example, Applicants submit that, as stated above, there exists no motivation to combine the teachings of Hebert with those of Zommer for at least the reason that Hebert contains no substantive teachings regarding the substrate layer, e.g., P+ substrate layer 10 in FIG. 1 and therefore it would be difficult to ascertain what actual breakdown voltage is present in Hebert and thus whether altering the breakdown voltage would even be desirable.

Further, Applicants submit that the cited references, even if combinable, do not teach or suggest each and every element of the claimed invention. Applicants again note that with regard

to the stated grounds of rejection set forth on page 2, 2nd paragraph, of the final Office Action, no rejection of claims 1-8 and 13-6 is made based on Sherman. Despite the Examiner's statement in the Advisory Action, page 2, 4th paragraph, with regard to claims 9-12 and Sherman (cited above), it is still unclear how the Examiner intended Sherman to apply to independent claim 16. Notwithstanding this ambiguity, Applicants respectfully submit that the combined teachings of Hebert, Zommer, Savastiouk and Sherman fail to teach or suggest each and every element present in independent claim 16.

Specifically, the combined teachings of Hebert, Zommer, Savastiouk and Sherman fail to teach or suggest a stress compensation layer that has a tensile stress that counterbalances at least a portion of the overall residual stress of the device, the overall residual stress of the device being attributable at least in part to a thinning process applied to the substrate. For example, nothing in the combined teachings of the cited references in any way indicates that the tensile stress of an SiO_2 film, e.g., as taught in Sherman, combined with the stress relief dielectric layer, e.g., as taught in Hebert, would be able to counterbalance any amount of stress resulting from substrate thinning, e.g., as taught in Zommer. This element, absent in the cited references, is only taught in the present teachings.

Further, the combined teachings of the cited references do not disclose an integrated circuit, as in independent claim 16. The Examiner seems to agree with this point by stating in the final Office Action, page 5, 2nd paragraph, that "Hebert does not explicitly disclose that the device is part of an integrated circuit." Therefore, for at least this reason, independent claim 16 is patentable over the cited references.

As such, independent claim 16 is patentable over Hebert, Zommer, Savastiouk and Sherman. Reconsideration and withdrawal of the rejections is thus respectfully requested.

2. §103(a) Rejection of Claims 9-12

Claims 9, 11 and 12

Applicants initially note that, with regard to Sherman, no rejection of independent claim 1 was made over Sherman. For example, as presented above, rejections based on a combination of teachings that included Sherman were made only in reference to independent claims 13 and

16. Applicants again point to the Advisory Action, page 2, 4th paragraph, wherein it was stated that,

> Applicant is correct in noting that Sherman was omitted in the caption, but was recovered in the caption for Claims 9-12. However, assertions of patentability based on the independent claims . . . is not warranted.

Thus, Applicants remain uncertain as to how the Examiner intended the teachings of Sherman to apply to claims 9-12, because no remarks were presented in the final Office Action or in the Advisory Action that are related to Sherman and claims 9-12. Clarification is thus respectfully requested.

Claim 9 specifies that the stress compensation layer applied to the surface of the device changes the curvature of the device.

The Examiner in the final Office Action, page 2, 3rd paragraph, stated that "Hebert discloses a method for controlling the curvature . . . of a device" (internal citations omitted). The Examiner also stated on page 5, 4th paragraph, of the final Office Action, that,

> [r]egarding Claims 9 and 10, Hebert does not disclose that the application of the stress compensating layer either maintains or alters the curvature of the device. Wilson et al. disclose that the stress in the structure will cause the wafer to bend and thus alter the curvature (internal citations omitted).

Applicants respectfully submit that there exists no motivation to combine the teachings of Hebert with those of Wilson. Specifically, contrary to the Examiner's above-cited assertions, nowhere does Hebert disclose curvature, or controlling curvature in a device. Further, Hebert does not contain any specific teachings regarding, e.g., the thickness of P+ substrate 10, and therefore it cannot be assumed, with any degree of certainty, that any amount of curvature occurs. For example, it is equally plausible, given the teachings in Hebert, that the P+ substrate is of a thickness such that no curvature is experienced, regardless of the stress in a layer deposited on the device.

To this point, the Examiner, in the Advisory Action, page 3, 4th paragraph, stated that,

> [w]ith regard to commentary of Applicant relating thicknesses of components and resultant stress Applicant is correct in stating that there are particular thicknesses wherein no curvature would be observed. However, this is not germane to the topic here, since the claims and the references assume there are thicknesses where curvature will occur (internal citations omitted)

Applicants respectfully disagree with the Examiner's assertions. Specifically, since, as stated above, Hebert does not disclose curvature of a device, it is not necessarily true that the "references assume there are thicknesses where curvature will occur." In fact, since curvature is not mentioned in Hebert, it is likely that device curvature is not a consideration, and is not assumed to occur.

Therefore, Applicants respectfully submit that one of ordinary skill in the art would find no motivation to combine the teachings of Hebert with those of Wilson, for at least the reason that Wilson is directed to device curvature and Hebert is not.

Applicants thus respectfully submit that claim 9 is patentable over the cited references. Reconsideration and withdrawal of the rejections is respectfully requested.

Claim 10

With regard to claim 10, this claim specifies that the stress compensation layer applied to the surface of the device maintains the curvature of the device. The Examiner in the final Office Action, page 5, 4th paragraph, stated that according to the teachings of Hebert and Wilson "optimization can be used to determine the values for thinning and film thickness to either maintain curvature or change curvature."

As stated above, for at least the reason that Wilson is directed to device curvature and Hebert is not, there exists no motivation to combine the teachings of Hebert with those of Wilson. Further, regardless of the teachings of the references alluded to by the Examiner allegedly describing device curvature, the references, even if combinable, do not in any way teach or suggest employing a stress compensation layer to maintain the curvature of a device. In fact, the teachings of Wilson are merely directed to determining the amount of bend experienced as a result of the stresses in a deposited thin film. Specifically, Wilson teaches simply "measuring the change in wafer curvature before and after the film deposition." Wilson, page 223, 2nd paragraph (emphasis added). Therefore, Wilson has absolutely nothing to do with maintaining, in any way, the curvature of a device.

Therefore, for at least the reasons stated above, claim 10 is patentable over the cited references. Reconsideration and withdrawal of the rejections is respectfully requested.

In conclusion, it is believed that the §103(a) rejections of claims 1-16 are improper and should be withdrawn.

In view of the foregoing, Applicants believe that claims 1-16 are in condition for allowance, and respectfully request the withdrawal of the §103(a) rejections.

Respectfully submitted,

Dated: June 27, 2005

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CLAIMS APPENDIX

1. (Original) A method for controlling curvature of a power transistor device comprising a device film formed on a substrate, the method comprising the steps of:

thinning the substrate, the device having an overall residual stress attributable at least in part to the thinning step; and

applying a stress compensation layer to a surface of the device film, the stress compensation layer having a tensile stress sufficient to counterbalance at least a portion of the overall residual stress of the device.

2. (Original) The method of claim 1, wherein the stress compensation layer comprises a thin film.

3. (Original) The method of claim 1, wherein the power transistor comprises a DMOS device.

4. (Original) The method of claim 1, wherein the device substrate is thinned using aggressive backside substrate removal processing.

5. (Original) The method of claim 2, wherein the thin film comprises a dielectric material comprising at least one of a silicon nitride, a silicon oxide, a silicon oxynitride, an oxynitride, a nitride and combinations comprising at least one of the foregoing dielectric materials.

6. (Original) The method of claim 2, wherein the thin film is applied using a deposition technique comprising at least one of sputtering, chemical vapor deposition, electroplating and spin-on processing.

7. (Original) The method of claim 1, wherein the steps of thinning and applying are performed repeatedly until a desired curvature is attained.

8. (Original) The method of claim 2, wherein the thin film serves as an encapsulating layer.

9. (Original) The method of claim 1, wherein the stress compensation layer applied to the surface of the device changes the curvature of the device.

10. (Original) The method of claim 1, wherein the stress compensation layer applied to the surface of the device maintains the curvature of the device.

11. (Original) The method of claim 1, further comprising the step of monitoring the curvature of the device.

12. (Original) The method of claim 11, wherein the curvature of the device is monitored using an off-axis optical laser technique.

13. (Original) A power transistor device comprising:

a substrate; and

a device film formed on the substrate, the device having an overall residual stress attributable at least in part to a thinning process applied to the substrate;

wherein the power transistor device further comprises a stress compensation layer formed on a surface of the device film, the stress compensation layer having a tensile stress that counterbalances at least a portion of the overall residual stress of the device.

14. (Original) The device of claim 13, wherein the stress compensation layer comprises a thin film.

15. (Original) The device of claim 14, wherein the thin film comprises an encapsulating layer.

16. (Original) An integrated circuit, comprising:

at least one power transistor device comprising a substrate and a device film formed on the substrate, the device having an overall residual stress attributable at least in part to a thinning process applied to the substrate;

wherein the power transistor device further comprises a stress compensation layer formed on a surface of the device film, the stress compensation layer having a tensile stress that counterbalances at least a portion of the overall residual stress of the device.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.

COPY

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Transmittal Letter – (Original & 1 copy)
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Case Name: Fratti 12-19
Serial No.: 10/628,941

1150-1133

April 21, 2005 (MJC)

PTO/SB/31 (02-01)
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NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional)
Fratti 12-19

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Signature: Tina Maurice

Typed or printed name: Tina Maurice

In re Application of: Fratti et al.

Application Number	Filed
10/628,941	July 29, 2003

For: Techniques for Curvature Control in Power Transistor Devices

Group Art Unit	Examiner
2811	Thomas J. Magee

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 1.17(b)) $500.00.

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $_____.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.

☑ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0762. I have enclosed a duplicate copy of this sheet.

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record.

☐ attorney or agent acting under 37 CFR 1.34(a). Registration number if acting under 37 CFR 1.34(a)._____.

Signature

Michael J. Chang
Typed or printed name

April 21, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Fratti et al.
Case: 12-19
Serial No.: 10/628,941
Filing Date: July 29, 2003
Group: 2811
Examiner: Thomas J. Magee

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: _____ Date: June 27, 2005

Title: Techniques for Curvature Control in Power Transistor Devices

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TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

1. Appeal Brief; and
2. Copy of Notice of Appeal, filed on April 21, 2005, with copy of stamped return postcard indicating receipt of Notice by PTO on April 25, 2005.

There is an additional fee of $500 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of $500, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully,

Date: June 27, 2005

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